Amendments to the Claims:

Claims 1-15 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, ~~said~~the semiconductor substrate including at least one opening extending therethrough between ~~said~~the semiconductor substrate first surface and ~~said~~the semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on ~~said~~the semiconductor die active surface, ~~said~~the at least one semiconductor die oriented having ~~said~~the at least one electrical connection area substantially aligned with ~~said~~the at least one semiconductor substrate opening; and

at least one piece of adhesive tape interposed between and attaching ~~said~~the semiconductor die active surface and ~~said~~the semiconductor substrate first surface, ~~a width of the one piece of adhesive tape extending at least one of to at least said edge of said at least one semiconductor substrate opening to provide a detectable surface within said at least one semiconductor substrate opening and at least to said edge of said at least one semiconductor die to provide a detectable adhesive tape surface on said semiconductor substrate first surface~~ a width of the at least one piece of adhesive tape extending beyond at least one of an edge of the at least one semiconductor substrate opening and an edge of the at least one semiconductor die to provide a detectable surface of the at least one piece of adhesive tape.

2. (Currently Amended) A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein ~~said~~the semiconductor substrate includes at least one opening defined therethrough between ~~said~~the semiconductor substrate first surface and ~~said~~the semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on ~~said~~the semiconductor die active surface, ~~said~~the at least one semiconductor die oriented having ~~said~~the at least one electrical connection area substantially aligned with ~~said~~the at least one semiconductor substrate opening, ~~said~~the electrical connection area disposed on ~~said~~the semiconductor die active surface, ~~said~~the at least one electrical connection area directly connected to at least one output electrical connection of ~~said~~the semiconductor device; and

at least one adhesive tape interposed between and attaching ~~said~~the semiconductor die active surface and ~~said~~the semiconductor substrate first surface, a width of ~~said~~the at least one adhesive tape extending at least proximate an edge of ~~said~~the at least one semiconductor die to an edge of ~~said~~the at least one semiconductor substrate opening, ~~said~~the width of ~~said~~the at least one adhesive tape extends beyond ~~said~~the edge of ~~said~~the at least one semiconductor substrate opening a distance into ~~said~~the at least one semiconductor substrate opening to provide a detectable surface within ~~said~~the at least one semiconductor substrate opening.

3. (Currently Amended) A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein ~~said~~the semiconductor substrate includes at least one opening defined therethrough between ~~said~~the semiconductor substrate first surface and ~~said~~the semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on ~~said~~the semiconductor die active surface, ~~said~~the at least one semiconductor die oriented having ~~said~~the at least one electrical connection area

substantially aligned with ~~said~~the at least one semiconductor substrate opening, ~~said~~ the at least one electrical connection area disposed on ~~said~~ the semiconductor die active surface, ~~said~~ the at least one electrical connection area directly connected to at least one output electrical connection of ~~said~~ the semiconductor device; and

at least one adhesive tape interposed between and attaching ~~said~~the semiconductor die active surface and ~~said~~the semiconductor substrate first surface, a width of ~~said~~the at least one adhesive tape extending at least proximate an edge of ~~said~~the at least one semiconductor die to an edge of ~~said~~the at least one semiconductor substrate opening and extending beyond ~~said~~the edge of ~~said~~the at least one semiconductor die a distance on ~~said~~the semiconductor substrate first surface to provide a detectable adhesive tape surface on ~~said~~the semiconductor substrate first surface.

4. (Currently Amended) The semiconductor die assembly of claim 1, further including at least one electrical connection extending between ~~said~~the at least one electrical connection area and at least one trace on ~~said~~the semiconductor substrate second surface.

5. (Currently Amended) The semiconductor die assembly of claim 4, wherein ~~said~~the at least one electrical connection comprises a bond wire.

6. (Currently Amended) The semiconductor die assembly of claim 4, wherein ~~said~~the at least one electrical connection comprises a TAB connection.

7. (Currently Amended) The semiconductor die assembly of claim 4, further including a glob top material disposed within ~~said~~the at least one semiconductor substrate opening encasing ~~said~~the at least one electrical connection.

8. (Currently Amended) The semiconductor die assembly of claim 7, further including an encapsulant material encasing ~~said~~the at least one semiconductor die and ~~said~~the glob top material.

9. (Currently Amended) The semiconductor die assembly of claim 1, wherein ~~said~~the at least one adhesive tape comprises a planar carrier film including a first surface having a first adhesive disposed thereon and a second surface having a second adhesive disposed thereon.

10. (Currently Amended) A semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein ~~said~~the semiconductor substrate includes at least one opening defined therethrough between ~~said~~the semiconductor substrate first surface and ~~said~~the semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on ~~said~~the semiconductor die active surface, ~~said~~the at least one semiconductor die oriented having ~~said~~the at least one electrical connection area substantially aligned with ~~said~~the at least one semiconductor substrate opening; and

at least one adhesive tape interposed between and attaching ~~said~~the semiconductor die active surface and ~~said~~the semiconductor substrate first surface, a width of ~~said~~the at least one adhesive tape extends at least proximate an edge of ~~said~~the at least one semiconductor die to an edge of ~~said~~the at least one semiconductor substrate opening, ~~said~~the at least one adhesive tape comprises a planar carrier film including a first surface having a first adhesive disposed thereon and a second surface having a second adhesive disposed thereon, and the composition of ~~said~~the first adhesive differs from a composition of ~~said~~the second adhesive for substantially preventing damage to a portion of the active surface of the semiconductor die by filler particles in a material used to fill the at least one opening in the substrate being located between the first surface of the substrate and the active surface of the at least one semiconductor die.

11. (Currently Amended) The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate ~~said~~the at least one adhesive tape and ~~said~~the edge of ~~said~~the at least one semiconductor die.

12. (Currently Amended) The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate ~~said~~the at least one adhesive tape and ~~said~~the edge of ~~said~~the at least one semiconductor substrate opening.

13. (Currently Amended) The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate ~~said~~the at least one adhesive tape and ~~said~~the active surface of ~~said~~the at least one semiconductor die.

14. (Currently Amended) The semiconductor die assembly of claim 1, further comprising at least one fillet located proximate ~~said~~the at least one adhesive tape and ~~said~~the semiconductor substrate first surface.

15. (Currently Amended) A computer comprising:

at least one semiconductor die assembly, ~~said~~the semiconductor die assembly comprising:

a semiconductor substrate having a first surface and a second surface, wherein ~~said~~the semiconductor substrate includes at least one opening defined therethrough between ~~said~~the semiconductor substrate first surface and ~~said~~the semiconductor substrate second surface;

at least one semiconductor die having an active surface with at least one electrical connection area disposed on ~~said~~the semiconductor die active surface, ~~said~~the at least one semiconductor die oriented having ~~said~~the at least one electrical connection area substantially aligned with ~~said~~the at least one semiconductor substrate opening; and

at least one piece of adhesive tape interposed between and attaching ~~said~~the semiconductor die active surface and ~~said~~the semiconductor substrate first surface, ~~a width of one piece of adhesive tape of the two pieces of adhesive tape extending at least one of at least to said~~

~~edge of said at least one semiconductor substrate opening to provide a detectable surface within said at least one semiconductor substrate opening and at least tosaid edge of said at least one semiconductor die to provide a detectable adhesive tape surface on said semiconductor substrate first surface~~ a width of the at least one piece of adhesive tape extending beyond at least one of an edge of the at least one semiconductor substrate opening and an edge of the at least one semiconductor die to provide a detectable surface of the at least one piece of adhesive tape.